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### Introduction

The MB650 debug board is designed for use with the NHK15 and features:

- An Ethernet interface
  - LAN91C113 Ethernet controller and an RJ45 connector
- An ARM JTAG
  - One JTAG connector for debugging purposes
- Four expansion connectors
  - Two expansion connectors for the NHK15 mother board
  - Two expansion connectors for external daughter boards
- A UART interface
  - A standard RS232 serial interface connector

# 1 Board layout

The debug board is a 4 layer board, its form factor is: 65 mm x 65 mm.

Figure 1. Board top side

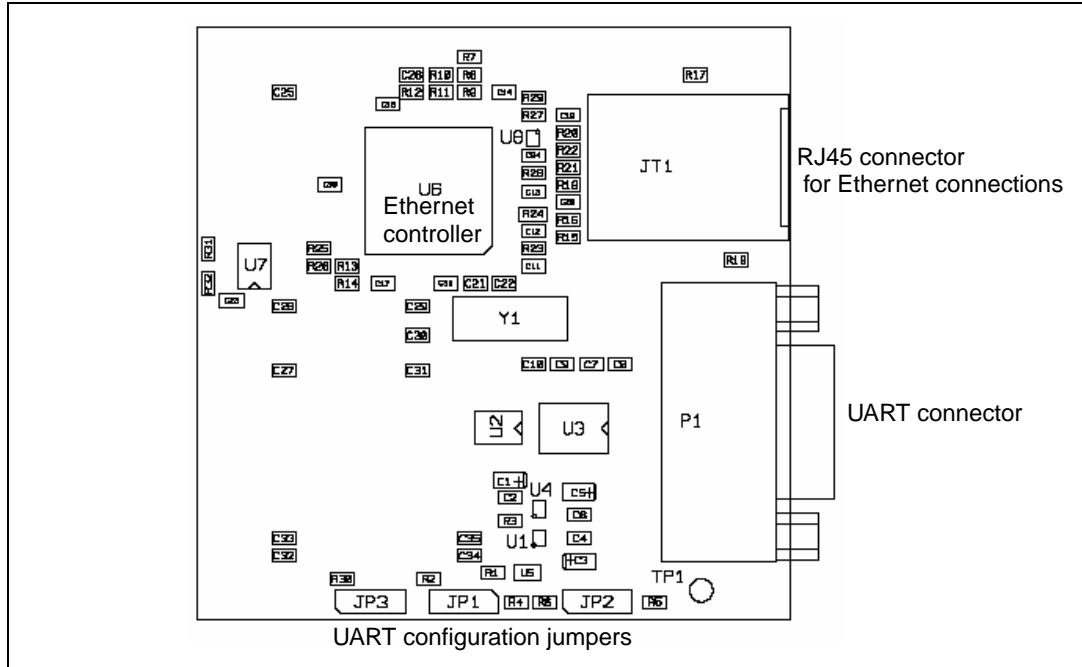
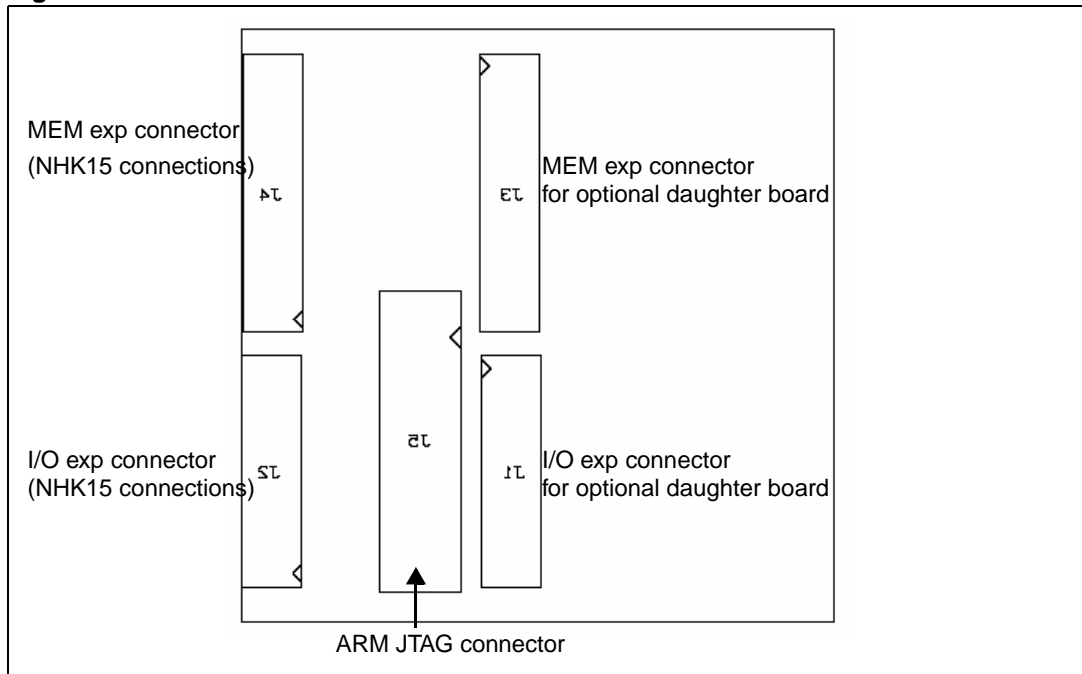


Figure 2. Board bottom side



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## 2 Ethernet (LAN91C113-NU)

The Ethernet controller LAN91C113-NU and the RJ45 connector (MIC24011-0101-LF3, with embedded transformer and activity LEDs) provide the Ethernet interface.

The LAN91C113-NU memory map device:

- provides fast Ethernet connectivity
- is a single chip Ethernet controller, dual speed 10/100 Mbps
- supports 8-bit and 16-bit CPU access
- supports fully integrated IEEE 802.3/802.3u-100Base-Tx/10 Base-T physical layer
- supports auto negotiation 10/100, full/half duplex
- package is TQFP 128

It is connected to the FSMC interface in the NOR chip select 1 address space. Data transfer can only be performed for 16-bit wide data in asynchronous mode. Memory mapping is 0x34000000 to 0x34FFFFFF.

Main connections:

- The LAN91C113 address bit and data bit are connected to the STn8815 muxed address/data bus SMADQ [15-0]; the addresses are latched internally to the controller by the SMADV signal.
- The interrupt signal (ETH\_INT) is controlled by NHK15 EXP1\_GPIO11, the signal is an edge trigger interrupt.
- The reset signal (ETH\_RESET) is controlled by NHK15 EXP1\_GPIO10. When set to 1, the signal keeps the LAN controller in reset mode.

**Table 1. Ethernet controller**

Device	SMSC1	SMAD24	SMAD23
Ethernet controller	0	0	0

## 3 RS232 interface

The debug board supports a standard RS232 serial interface (9 poles RS232 connector), which can be used for the following NHK15 board interfaces:

- Bluetooth UART interface (STn8815 UART0), for external Bluetooth download
- STn8815 UART1 interface, for debugging and toolset download

Only one interface at a time can be used, JP1 and JP2 select one of two interfaces:

**Table 2. UART interface selection using jumpers**

Interface selection	JP1	JP2
RS232 enabled to Bluetooth UART0	2-3 closed	not relevant
RS232 enabled to UART1	1-2 closed	1-2 closed
Enable MSP3 to UART1	1-2 closed	2-3 not relevant

## 4 ARM JTAG

The debug board can be used for ARM debug features via the on-board JTAG connector (J5 FAP-10X2P-MALE) located on the top side of the board; see [Figure 1](#).

The JTAG connector has all the required signals for ARM debugging, the NHK15 mother board has all the pull-up (at 1.8V) and pull-down resistors.

## 5 Expansion connectors

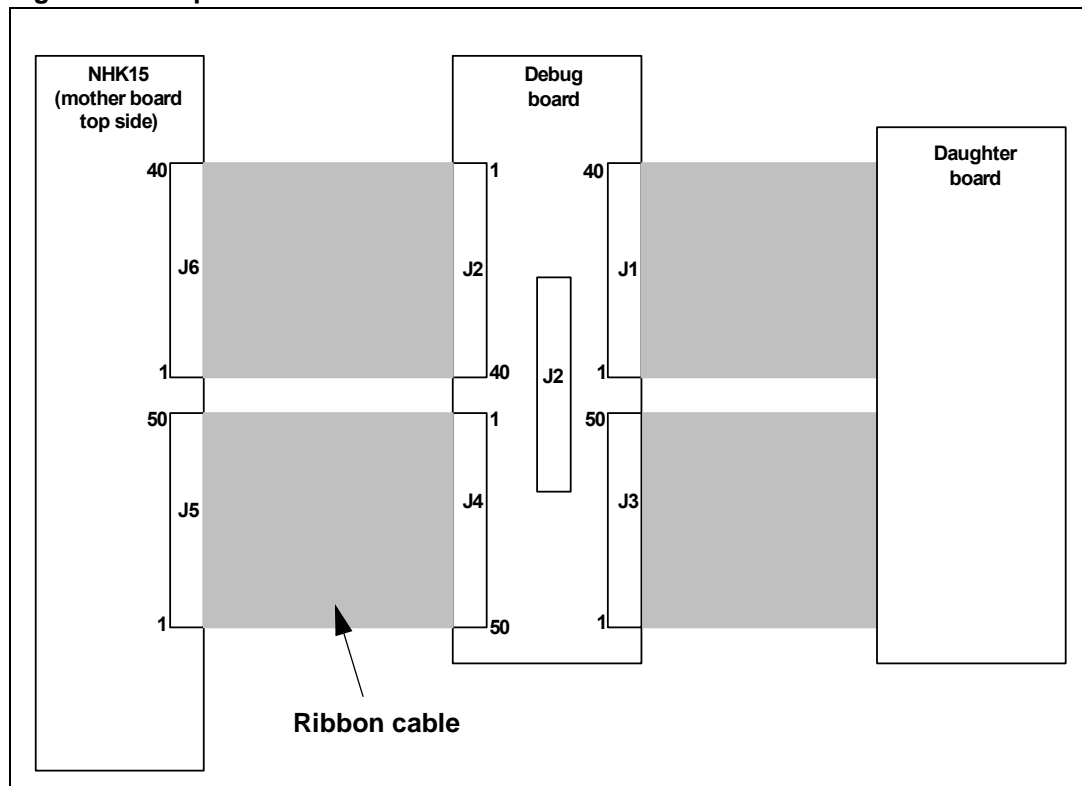
The debug board includes four expansion connectors:

- Two memory expansion connectors, J3, and J4 (Molex SMD connector 50 poles FEM 90° 54132-5097 LF)
- Two I/O expansion connectors, J1 and J2 (Molex SMD connector 40 poles 54132-4097 LF)

These connectors can be used as shown in [Figure 3](#).

- Connectors J4 and J2 connect to the NHK15 mother board via a ribbon cable.
- Connectors J3 and J1 connect daughter boards to the NHK15 when the debug board is being used.

**Figure 3. Expansion connectors**



## 5.1 Memory expansion connectors (J3 and J4)

As shown in [Figure 3](#), J4 connects the debug board to the NHK15 board, whilst J3 is available for optional daughter boards. A daughter board connected to J3 can be selected in the address range shown in [Table 3](#).

**Table 3. Address range of the daughter board connected to J3**

Chip select	Address range	SMAD24-23	Device
SMCS1n	0x35000000 to 0x35FFFFFF	0,1	Available for daughter boards
	0x36000000 to 0x36FFFFFF	1,0	
	0x37000000 to 0x37FFFFFF	1,1	
SMPS1n	0x5000 0000 to 0x5FFF FFFF	n.a	Available for daughter boards

**Table 4. Memory expansion connectors pinout**

J4 pin	J3 pin	Signal name	Level	Feature
50	1	V_1V8	1.8V	Power
49	2	V_1V8	1.8V	Power
48	3	GND		Ground
47	4	SMAD_3V3_24	3.3V	These two signals (address line 24 & 23) select the address range in the NOR chip select 1.
46	5	SMAD_3V3_23	3.3V	
45	6	SMAD_22	1.8V	GPIO116/SMAD22 available for optional daughter board. Can be used as GPIO or as memory address
44	7	SMAD_21	1.8V	GPIO115/SMAD21 available for optional daughter board. Can be used as GPIO or as memory address
43	8	SMAD_20	1.8V	GPIO114/SMAD20 available for optional daughter board. Can be used as GPIO or as memory address
42	9	SMAD_19	1.8V	GPIO113/SMAD19 available for optional daughter board. Can be used as GPIO or as memory address
41	10	SMAD_18	1.8V	Reserved for camera module
40	11	SMAD_3V3_17	3.3V	Memory address line 17
39	12	SMAD_3V3_16	3.3V	Memory address line 16
38	13	GND		Ground
37	14	GND		Ground
36	15	SMADQ_15	3.3V	Muxed address/data lines(15-9)
35	16	SMADQ_14	3.3V	
34	17	SMADQ_13	3.3V	
33	18	SMADQ_12	3.3V	
32	19	SMADQ_11	3.3V	
31	20	SMADQ_10	3.3V	
30	21	SMADQ_9	3.3V	

Table 4. Memory expansion connectors pinout (continued)

J4 pin	J3 pin	Signal name	Level	Feature
29	22	SMADQ_8	3.3V	Muxed address/data lines(8-0)
28	23	SMADQ_7	3.3V	
27	24	SMADQ_6	3.3V	
26	25	SMADQ_5	3.3V	
25	26	SMADQ_4	3.3V	
24	27	SMADQ_3	3.3V	
23	28	SMADQ_2	3.3V	
22	29	SMADQ_1	3.3V	
21	30	SMADQ_0	3.3V	
20	31	GND		Ground
19	32	ExpGPIO1	1.8V	Available for optional daughter board. Connect to NHK15 EXP1_GPIO12.
18	33	SMPS1n_3V3	3.3V	GPIO119/SMPS1n available for optional daughter board. Can be used as input only GPIO or as Memory chip select.
17	34	SMCS1n_3V3	3.3V	NOR address space chip select 1
16	35	SMWAITn	3.3V	FSMC wait signal
15	36	ETH_INT	1.8V	Ethernet interrupt (EXP1_GPIO11)
14	37	SMADVn_3V3	3.3V	Address valid signal. When low indicates that addresses are valid on SMADQ bus.
13	38	GND		Ground
12	39	SMWEn_3V3	3.3V	FSMC write enable. Active low.
11	40	SMOEn_3V3	3.3V	FSMC Output Enable. Active low.
10	41	ETH_RST	1.8V	Ethernet reset (EXP1_GPIO10)
9	42	GND		Ground
8	43	V_3V3	3.3V	Power
7	44	V_3V3	3.3V	Power
6	45	ExpGPIO2	1.8V	Available for optional daughter board. Connect to NHK15 EXP1_GPIO13
5	46	V_1V8	1.8V	Power
4	47	PORn	1.8V	Power on reset. Active low.
3	48	GND		Ground
2	49	V_3V3	3.3V	Power
1	50	V_3V3	3.3V	Power

## 5.2 I/O expansion connectors interfaces (J1 and J2)

These connectors carry the serial interface signals for UART, SSP, and I2C. Four GPIOs are also available plus JTAG signals. J2 connects to the NHK15 mother board, J1 connects to optional daughter boards.

**Table 5. J1 and J2 pinout**

J2 pin	J1 pin	Signal name	Level	Feature	Note
40	1	V_1V8	1.8V	Power	
39	2	V_1V8	1.8V		
38	3	UTXD1(MSPTXD3)	1.8V	STn8815 UART1 or MSP3 interface (GPIO56,52,57,51)	If serial bus (UART1 or MSP3) is used by optional daughter board, the jumper JP2 must have pin 2 and 3 closed.
37	4	URTS1(MSPTCKD3)	1.8V		
36	5	URXD1(MSPRXD3)	1.8V		
35	6	UCTS1(MSPTFS3)	1.8V		
34	7	GND	Ground		
33	8	BT_UTXD0	1.8V	STLC2590 UARTTX or STn8815 UART0 RX	If this serial bus is used by optional daughter board, the jumper JP1 must have pin 1 and 2 closed.
32	9	BT_URTS0	1.8V	STLC2590 UART RTS or STn8815 UART0 CTS	
31	10	BT_URXD0	1.8V	STLC2590 UARTRX or STn8815 UART0 TX	
30	11	BT_UCTS0	1.8V	STLC2590 UART CTS or STn8815 UART0 RTS	
29	12	GND	Ground		
28	13	SSPTXD	1.8V	STn8815 SSP interface	The SSPFRM on daughter board must be enabled only when ENSSP is = 0.
27	14	SSPRXD	1.8V		
26	15	SSPFRM	1.8V		
25	16	SSPCLK	1.8V		
24	17	ENSSP	1.8V	EXP0_GPIO17 must =0 to enable SSP	
23	18	GND	Ground		
22	19	I2CSDA	1.8V	STn8815 I2C0 interface	See <i>NHK15 user manual NM786</i> to check the available I2C address
21	20	I2CSCL	1.8V		
20	21	GND	Ground		
19	22	GPIOx0	1.8V	GPIO from STMPE2401 (STMPE1) (EXP1_GPIO14,15,16,17,18) available for daughter boards	
18	23	GPIOx1	1.8V		
17	24	GPIOx2	1.8V		
16	25	GPIOx3	1.8V		
15	26	GPIOx4	1.8V		


**Table 5. J1 and J2 pinout (continued)**

J2 pin	J1 pin	Signal name	Level	Feature	Note
14	27	GND	Ground		
13	28	Not connected		Reserved	Connected to pin 2 of JP3
12	29	JTAG_TCK	1.8V	STn8815 JTAG interface	The JTAG interface is not available on the J1 connector
11	30	JTAG_TDI	1.8V		
10	31	JTAG_TRSRTn	1.8V		
9	32	JTAG_TMS	1.8V		
8	33	JTAG_TDO	1.8V		
7	34	JTAG_RTCK	1.8V		
6	35	JTAG_SRSTn	1.8V		
5	36	V_1V2	1.2V	Power	
4	37	V_3V3	3.3V		
3	38	V_3V3	3.3V		
2	39	V_3V3	3.3V		
1	40	V_3V3	3.3V		

## 6 Jumper configuration

The debug board has three jumpers.

**Table 6. Jumpers default configuration**

Board ref.	Default configuration	Function	
JP1	1-2 closed	Enable UART1	
JP2	1-2 closed		
JP3	1-2 closed	reserved	



## 7 Revision history

Table 7. Document revision history

Date	Revision	Changes
22-June-2007	1	Initial release.

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